

Sony Smart-Kameras XCI



... Bildverarbeitungssystem in einer Kamera!

Features

Kamera-Features

- ✓ Video Output: 8,10 bit; S/W und Farbe
- ✓ VGA, SXGA
- ✓ 30, 90 fps
- ✓ Binning (2x2), Partial Scan
- ✓ Auto Gain Control
- ✓ Auto White Balance
- ✓ Auto Iris Control
- ✓ Umfangreiches SDK

Betriebssystem

- ✓ Microsoft Windows XP Embedded
- ✓ Linux



Design

- ✓ Kompaktes System: 94x70x140mm; 760 g
- ✓ C und CS-Mount
- ✓ Hohe Schock- (70G) und Vibrationsresistenz (10G bei 20 - 200Hz)
- ✓ Spannungsversorgung: 12V oder 24V
- ✓ Mehrere Schnittstellen

Leistungsmerkmale

- ✓ 1 GHz x86-compatible CPU (VIA Eden ULV; MMX, SSE, SSE2, SSE3)
- ✓ Xilinx Vertix-5- FPGA (SX35T: S/W; SX50T: Farbe)
- ✓ Hauptspeicher: 512 MB DDR2 SDRAM
- ✓ Compact-Flash: 1 bis 8 Gbyte
- ✓ VIA-Chipsatz

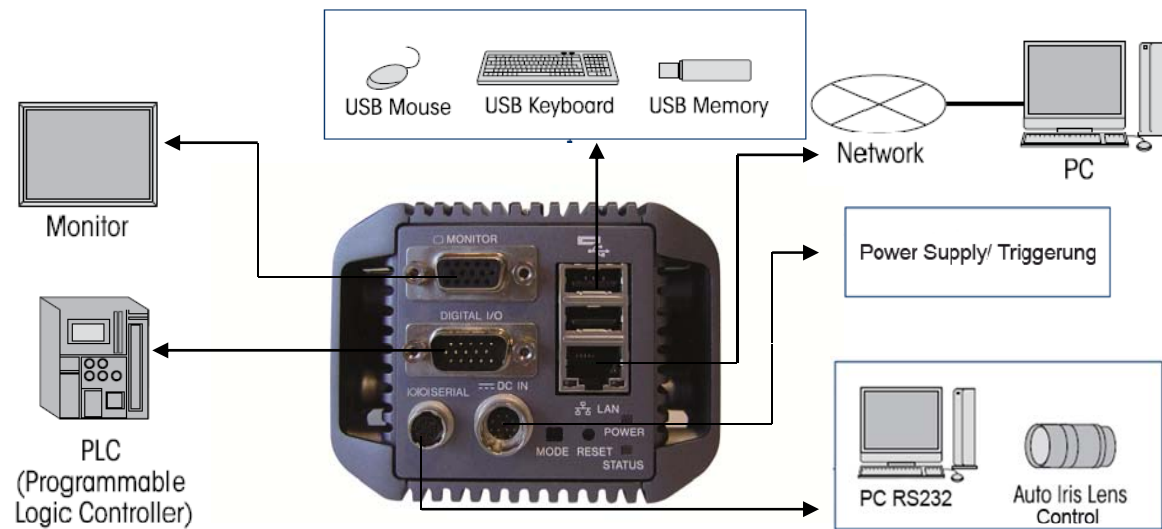
Modellübersicht



Modell	Sensor	Pixelgröße	Auflösung	Frames/s	Dim. (BxHxL)
Sony XCI-V100	1/3" HAD PS IT CCD	7.4 (µm)	640x480 (VGA)	90 fps	94x70x140 mm
Sony XCI-SX100	1/3" HAD ExView PS IT CCD	3.75 (µm)	1280x960 (SXGA)	30 fps	94x70x140 mm
Sony XCI-V100C	1/3" HAD PS IT CCD	7.4 (µm)	640x480 (VGA)	90 fps	94x70x140 mm
Sony XCI-SX100C	1/3" HAD ExView PS IT CCD	3.75 (µm)	1280x960 (SXGA)	30 fps	94x70x140 mm

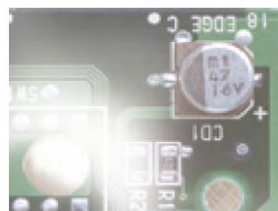
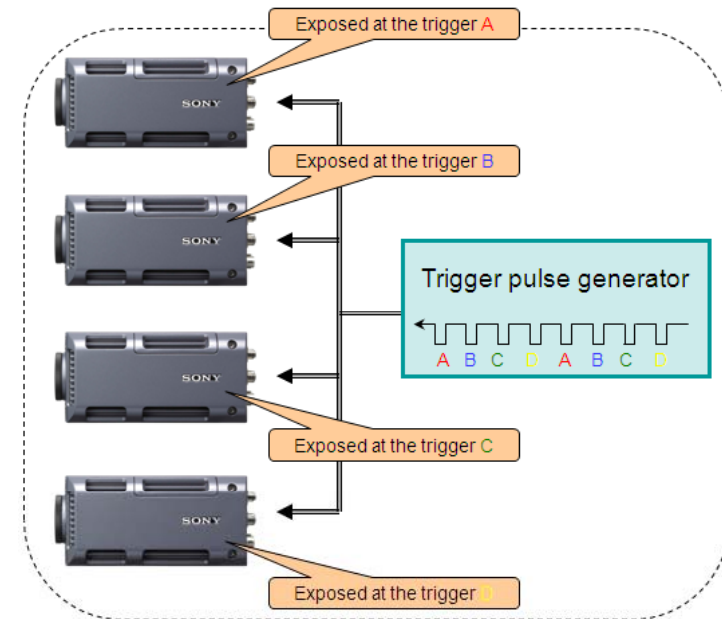
Schnittstellen

- ✓ VGA-Monitor-Anschluss (D-sub 15-pin)
- ✓ Gigabit Ethernet-LAN-Anschluss (1000,100,10 Base-T)
- ✓ 2x USB 2.0-Anschluss
- ✓ RS232-Anschluss; Auto-Iris (Lens Control)
- ✓ 4x ISO Input
- ✓ 8x ISO Output
- ✓ Reset-Schalter
- ✓ Status- und Power-LED

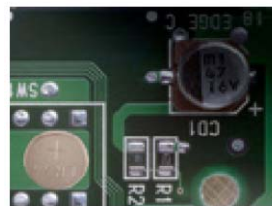


Hardware-Funktionen

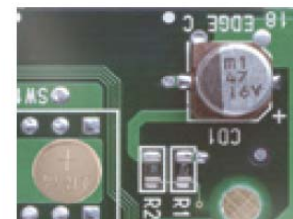
- ✓ Built-in real-time 5 x 5 image pre-processing filter
- ✓ Built-in 10 bit Hardware LUT (Look Up Table)
- ✓ Built-in Color-Processing
- ✓ Watch Dog Timer¹, SiSmart²
- ✓ **Shared Trigger**
- ✓ Dual Readout bei Wide-D Technology³



Slow Shutter Speed



High Shutter Speed



Composite Image with Wide-D Technology

1) Überwachungsfunktion, die beim Auftreten von Hardwarefehlern einen automatischen Reboot einleitet.
 2) Integrierte Überwachung von Lese- und Schreibvorgängen der Speicherkarten (nur mit Silicon Systems Karten).
 3) Wide-D: um ein Bild mit höherer Dynamic Range zu erhalten, können 2 Bilder mit unterschiedlichen Shutter-Geschwindigkeiten aufgenommen und anschließend überlagert werden.

Windows XPe

"Do it Yourself"

Hardware only solution (w/o CF
Windows XPe Licence)



Smartcam
SDK

Windows XPe

"Easy to use"

Camera hardware + software



+

Windows XPe

Accessory



1-8 GB CF
Embedded

with
Windows XPe licence
+ XPe driver
+ Sample application

"Flexible with software partners"

Camera hardware + software



+



+

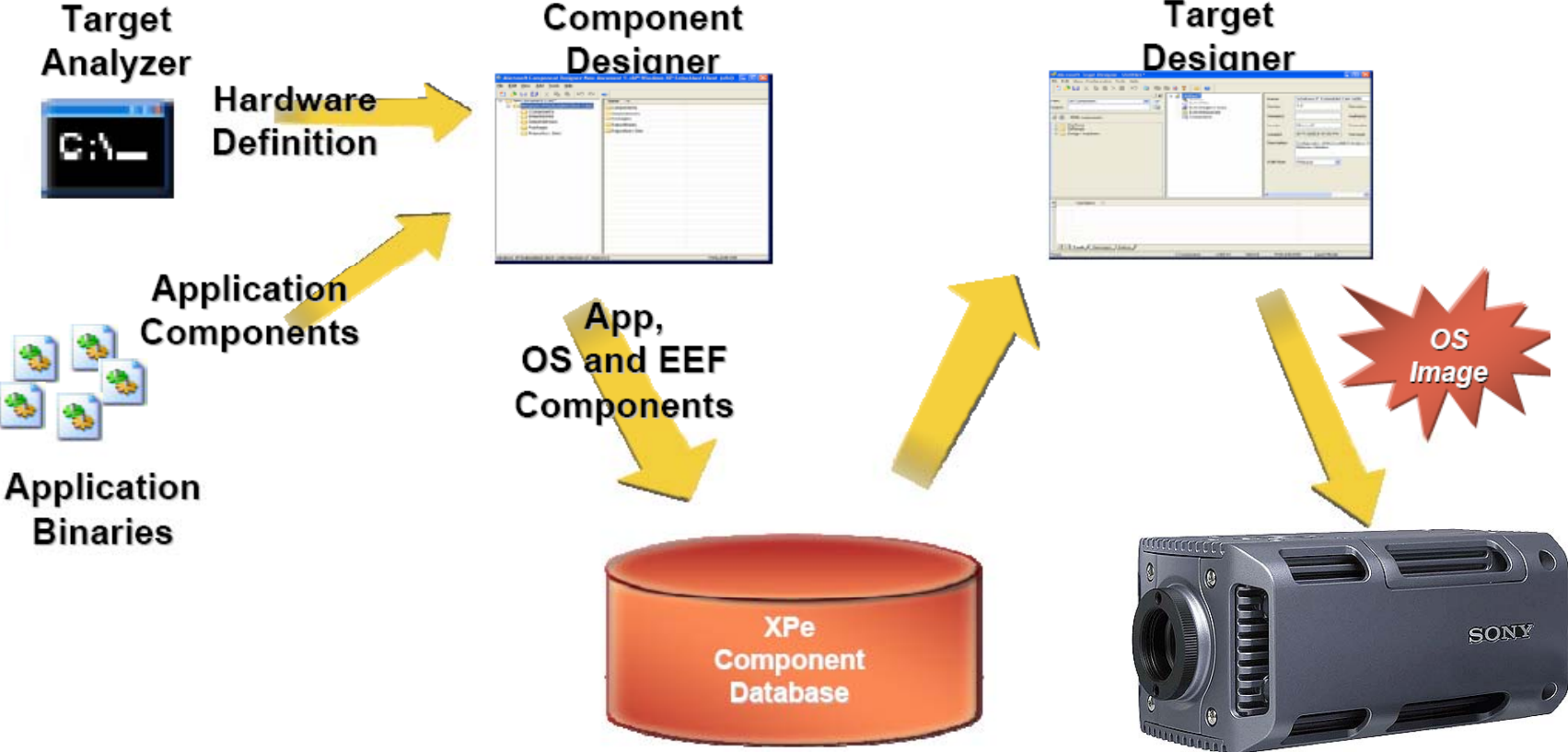
Windows XPe

Compatibility with partners

Machine Vision
Library/end-user
software

Security
Surveillance
Software

Windows XPe "Do it Yourself"



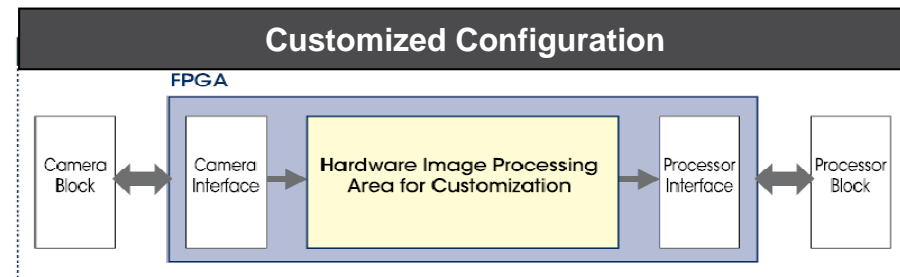
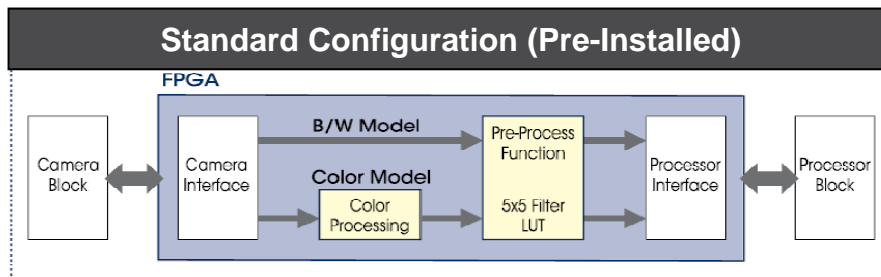
Software-Kompatibilität



Sony Compatibilty	Yes	Yes	Yes	Yes	Yes	Yes	TBC	TBC
Brand	MVTec	Matrox	National Instruments	Euresys	Cognex	Tordivel	NeuroCheck	Dalsa
Country	Germany	Canada	US	Belgium	US	Norway	Germany	Japan
Software Name(s)	Halcon ActivisionTools	MIL Lite MIL Inspector	LabView VBAI	Open eVision eVision	VisionPro QuickBuild	Scorpion	NeuroCheck	Sapera
Software Type	Library End User	Library	Library End User	Library	Library End User	End User	End User	Library
Capture SDK	Yes	No	Yes	No	Yes	No	No	No
Acquisition Support	Full integration validated by MVTec	Buffer mode	Buffer mode	Buffer mode (app note provided)	Full integration validated by Cognex	Full integration validated by Tordivel	Buffer mode (TBC)	Buffer mode (TBC)
Compatible Version(s)	Halcon 9.0 ActivisionTools 3.2	Mil 9.0	LabView 8.5 VBAI 3.5	Open eVision 1.0 eVision 6.7.1	VisionPro 5.2	Scorpion 6.0		

Customizable Open FPGA

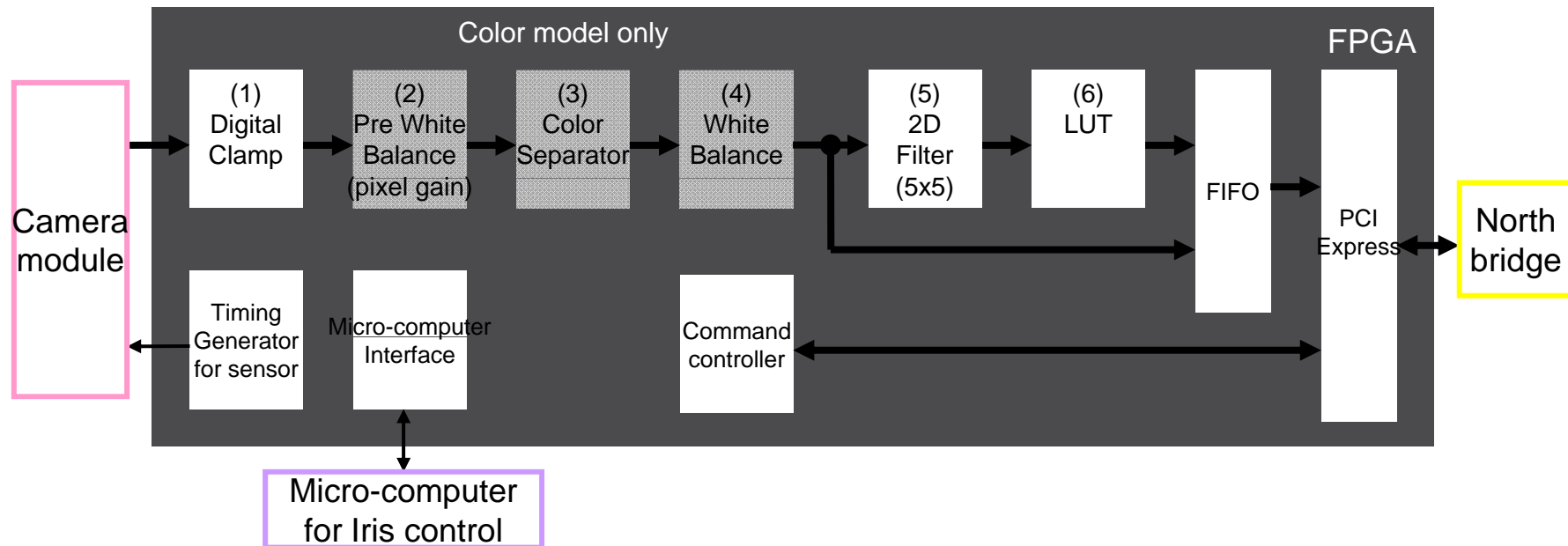
- ✓ Dynamisch programmierbar
- ✓ Verarbeitung von Rechenoperationen und Echtzeitprozessen
 - ➔ Entlastung der Host-CPU
 - ➔ Kamera wird schneller und leistungsstärker
- ✓ vorinstallierte Features (z.B. 5x5 Filter, Look Up Tables)
- ✓ eigene Algorithmen verwendbar
- ✓ verarbeitete und unverarbeitete Bilder gleichzeitig über die CPU und den FPGA abwickeln



FPGA "Hardware"

- ✓ Device: Xilinx Virtex-5
 - **XC5VSX35T** for B/W models
 - **XC5VSX50T** for Color models

- ✓ FPGA Block diagram



FPGA "Tools"

✓ Tools for FPGA modification

– **Necessary software**

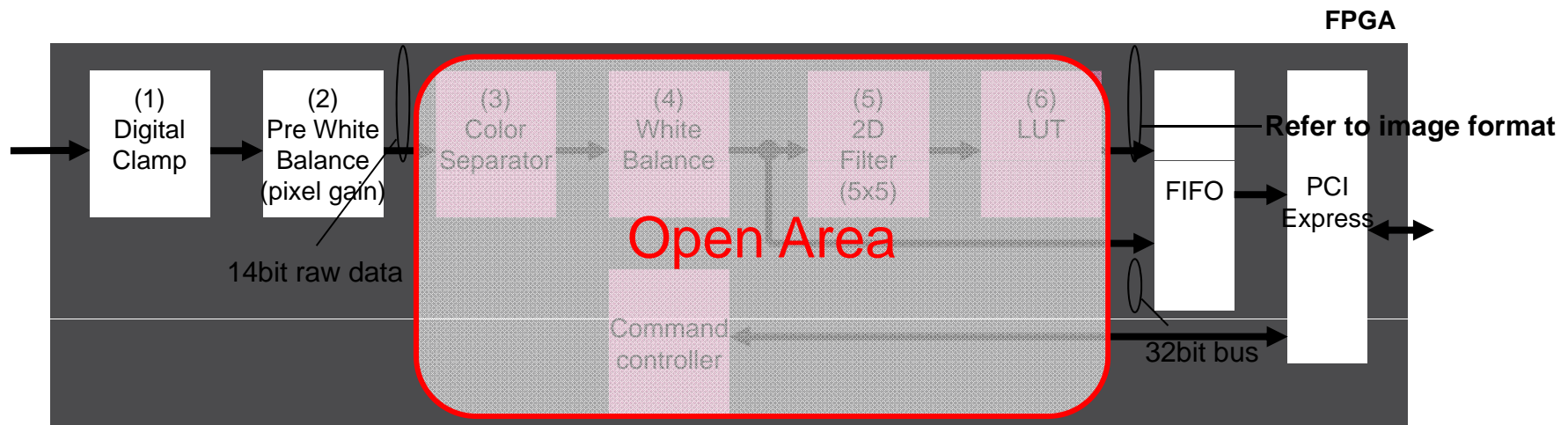
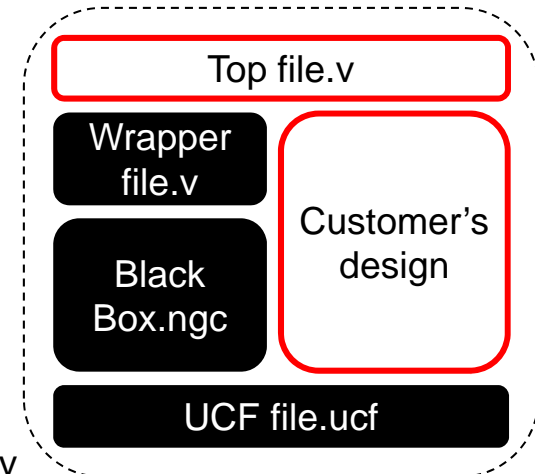
- ISE (Xilinx) (Recommended Version: Ver. 9.2)
- S/W writing FPGA data

– **FPGA pieces to be supplied from Sony**

- Reference Top file (.v) : Verilog top file
- Wrapper file (.v) : Verilog header file
- User Constraints File (.ucf) : Rule the pin assignment
- NET file (.ngc) : Black Box, Designed file by Sony

– **Interface (Black Box ↔ Open Area)**

On Xilinx's ISE



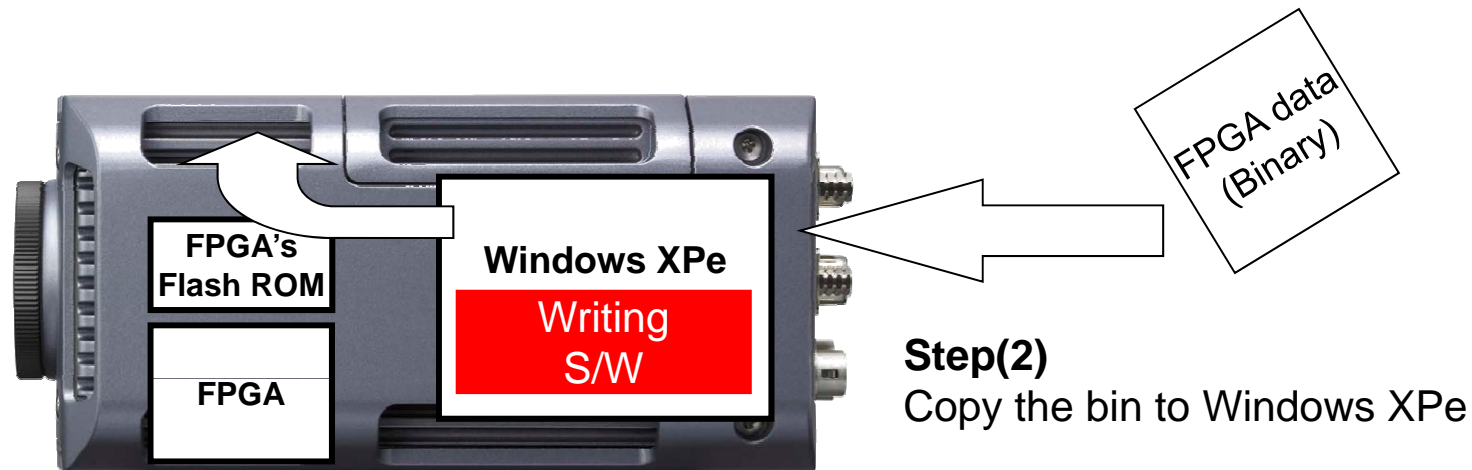
FPGA "Update"

Step(4)

Write the data to the flash ROM

Step(1)

Design FPGA data and make bin file



Step(2)

Copy the bin to Windows XPe

Step(3)

Install Sony's original writing S/W

Step(5)

Hardware restart