

ProCHILs™

Simulink® Simulation Acceleration Tool

Overview

GiDEL ProCHILs™ is a hardware acceleration tool that enables running **Simulink®** designs on high performance, powerful parallel FPGA hardware architecture.

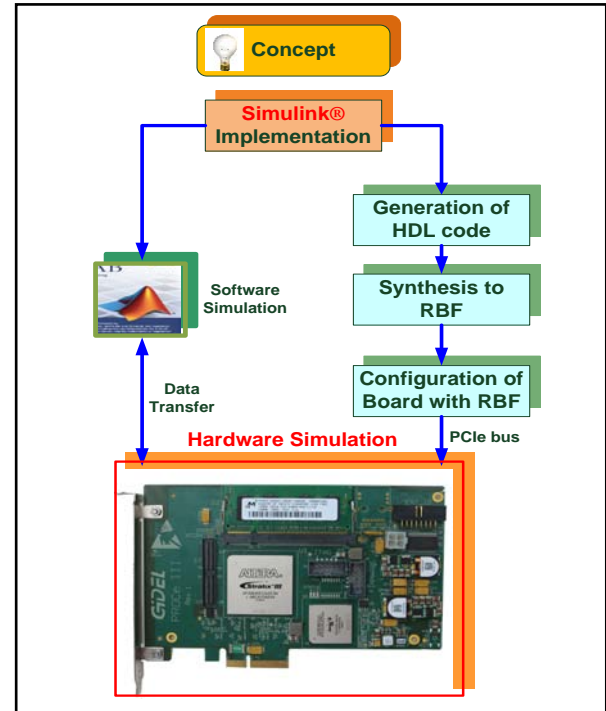
Simulink enables building and simulating complex model-based designs using an interactive graphical environment. However, the **Simulink** software simulation uses extensive PC resources and becomes significantly slower as the designs become more complex. Therefore, for multi-domain dynamic complex models, Simulation acceleration is vital.

The *GiDEL Proc* boards provide high-capacity, high-speed super accelerators based on FPGA reconfigurable computing. Using *ProCHILs*, Simulink designs may be compiled and downloaded into the Proc boards' FPGAs. To ensure maximum performance, *ProCHILs* connects **Simulink** to the Proc board via the PCIe bus. The *ProCHILs* can also interface via *Ethernet* with the *GiDEL ProcSoC* FPGA platform, thus enabling multiple remote users simultaneously.

The *ProCHILs* compiled designs run on the FPGAs and are fully controlled from within the user's natural **Simulink** environment. This enables tremendous ease of use and immediate significant reduction in simulation time.

ProCHILs Key Features

- Requires no programming knowledge whatsoever.
- Fully automatic code generation and downloading into FPGA.
- Data transfers to / from FPGAs using DMA to ensure optimal performance.
- Flexible board architecture that enables adding daughterboards to provide additional interfaces, such as **DVI**, **SDI** and **Camera Link**.
- Multiple-user **Ethernet** accessibility using the *ProcSoC* FPGA platform.
- Intuitive user-friendly interface that enables controlling the generation process at any stage to add HDL code to the generated logic.
- Supports DSP Builder® and Simulink® HDL Coder generation tools



ProCHILs Design Flow

ProCHILs Application Examples

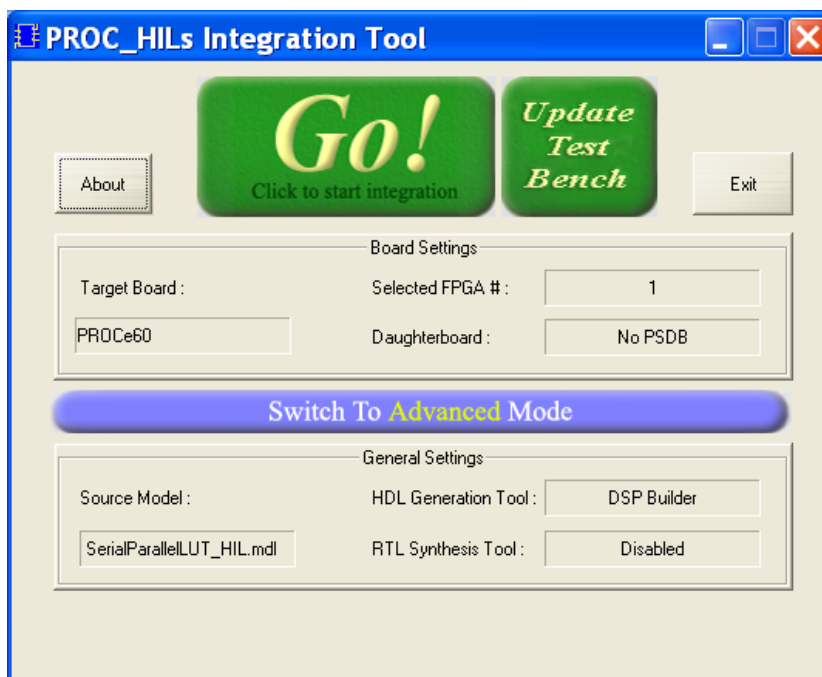
- Rapid prototyping
- System hardware acceleration
- Algorithm design and verification
- DSP

ProCHILs Benefits

- Dramatically improves simulation speed
- Combines the power and convenience of a visual development tool with the speed of a hardware design
- Enables building a design visually and downloading it directly into the FPGA Proc board.
- Design and configuration flexibility to accommodate user's needs
- Cuts development cycle time and budget while improving design reliability

Integration Process Flow Description

Accelerating simulation of Simulink models with the *ProcHILs* is a simple and intuitive procedure. Within a few effortless steps your model can be accelerated by tenfold factor: The model is built in **Simulink**, the design or part of the design runs on the on-board FPGAs, and the communication with the **Simulink** is in real-time and unnoticeable to the user. The whole generation process is fully automatic.



ProcHILs Integration Tool using **DSP Builder**®

The *ProcHILs* design flow includes the following simple steps:

- 1. Building a Simulink Design:** DSP Builder® or Simulink® HDL Coder blocks are used to build a model.
- 2. Inserting a Proc_HILs block:** Double clicking on the block opens the Proc_HILs Integration Tool.
- 3. Clicking “Go” to automatically generate and integrate:** During the integration process, an HDL code is generated from a Simulink design, synthesized and compiled to get an .rbf file (FPGA raw binary file) compatible with the Proc board. Proc_HILs runs all the tools that are necessary for this fully automated process.

When the generation process ends, a new Simulink design is generated. This design will contain a Proc_HILs block including all inputs and outputs, and connections to peripheral sources and sinks that were present in the original design.

- 4. Running an Accelerated Simulation:** The Proc_HILs automatically loads the .rbf file into the board and performs all necessary communications to execute the design in hardware. The design will run in full synchronization with Simulink, receiving the signals from the simulation sources and outputting the results into the sinks.

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