## PROC_HILs - Intuitive FPGA Use

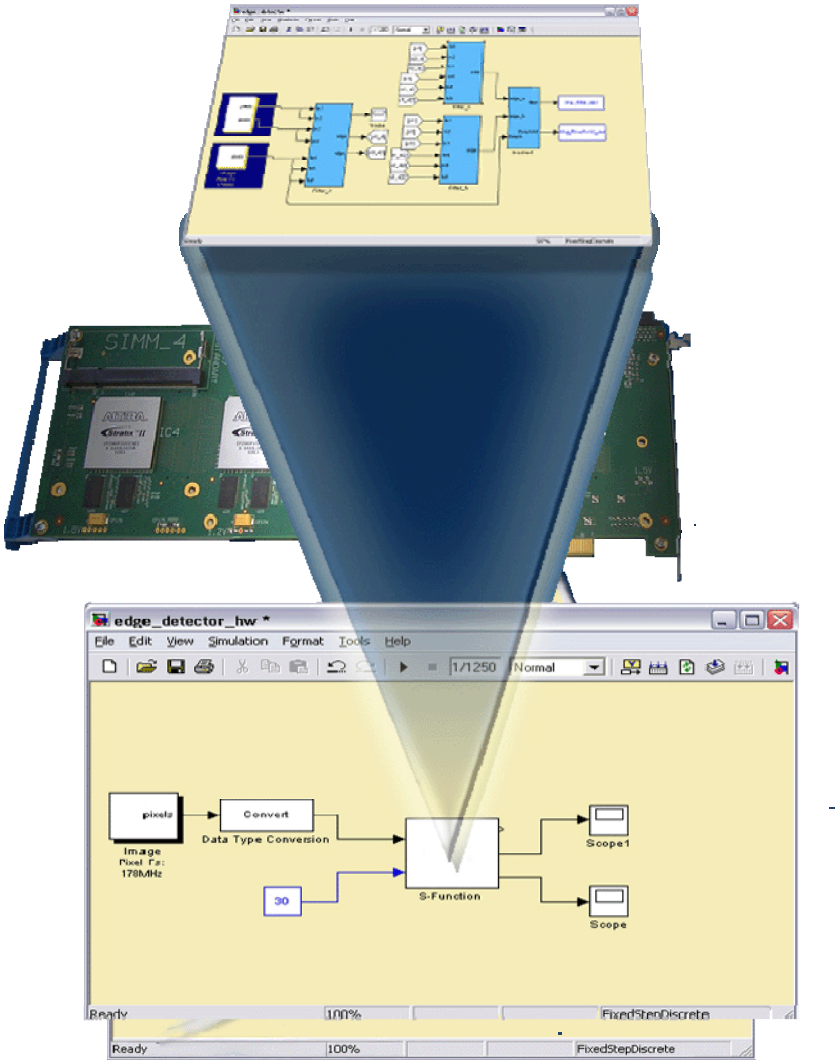
- Minimum effort: Push button process (integrated with partners' tools)
- Keep your design environment
- Accelerate performance by running your design in FPGA

# High System Performance

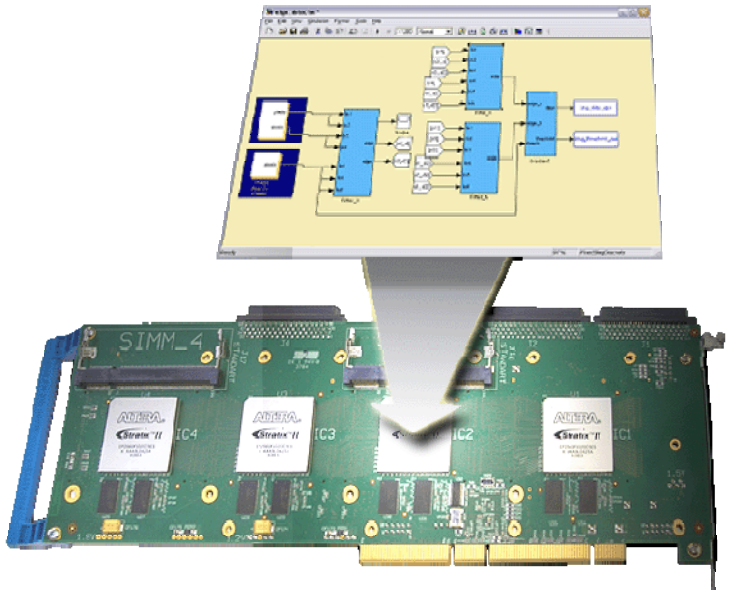
- Maximize performance
- Easily integrated into system
- Reliable, maintainable, upgradeable

# H I L Concept

## Accelerate Simulink simulations



# PROC_HILs Preparation Phase

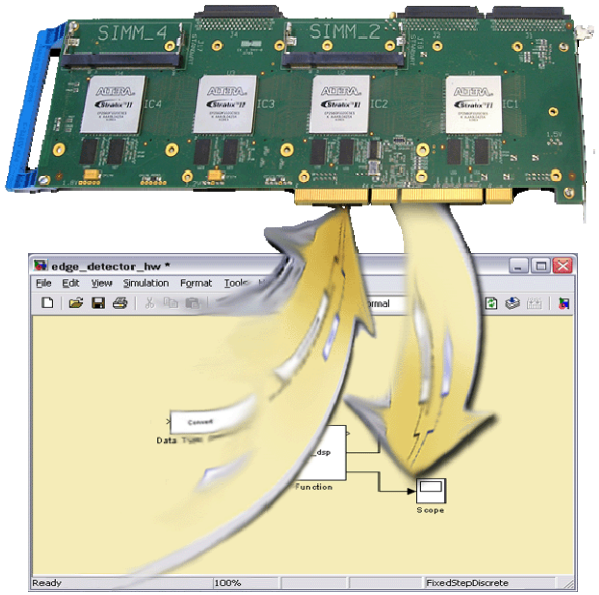



## Generate replacement design using FPGA

- Translate high level design into HDL
- Add GiDEL's Host IF & IPs
- Synthesize, place & route → **RBF**
- Generate design replacement

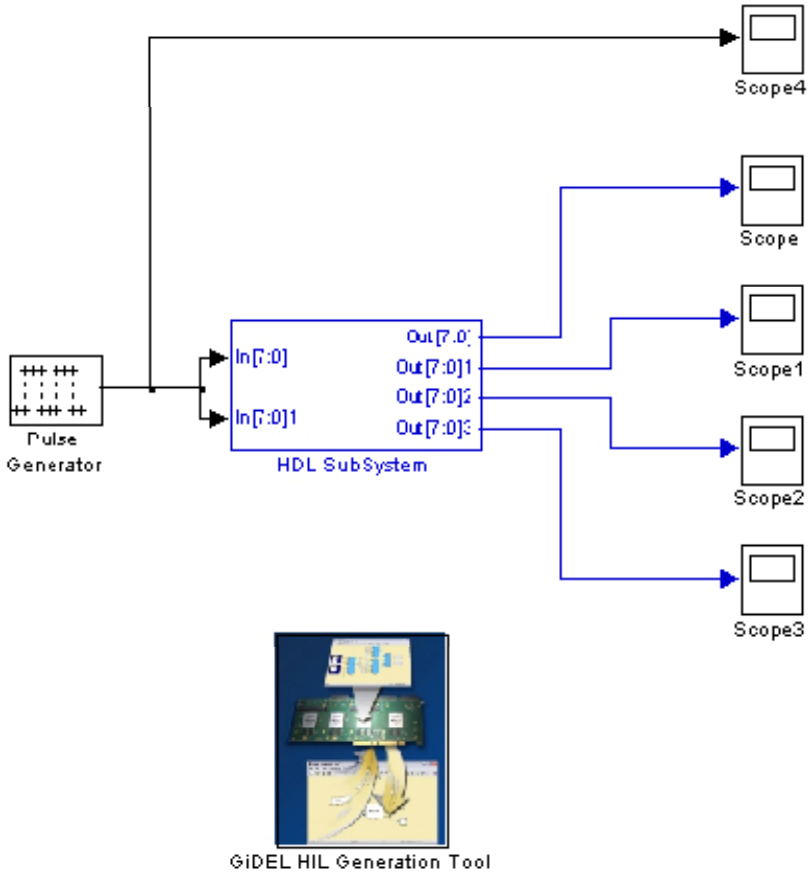
  → **S- function / C++ class**

# PROC_HILs Run Time




- Run original environment.
- Use the generated block as a design replacement.
- The design will use FPGA at “0 time”.
- (Advanced mode) Make some manual changes for system performance.

# Original Design



# PROC_HILs Generation Process

Press



Original Simulink Design
HDL Code
Optional: VQM Code

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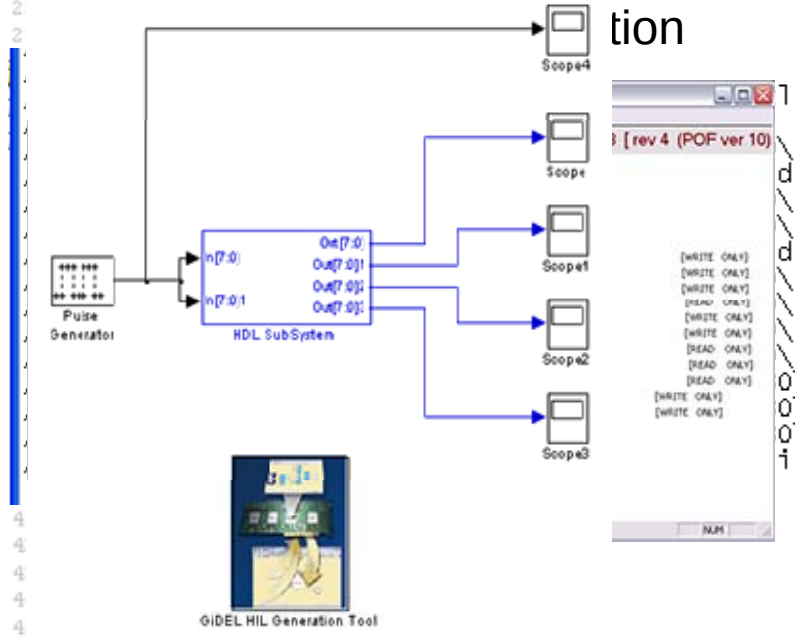

# Design After Generation