

Proc104™

Industrial PCIe/104™ FPGA Computation Accelerator

Key Features

- Altera Stratix IV 530-2 and 820-3, and Altera Stratix III 110E-3, 150L-3, 260E-2 FPGAs
- PCIe/104 form factor for Industrial applications
- 4-lane PCI Express (PCIe x4) host interface
- Five level memory structure (8.5 GB+).

Maximum sustained throughput of **4,693 GB/s** for internal memories and **12 GB/s** for DRAMs as follows:

- Up to 1280 M9K (9K-bit) DPRAM blocks
 - Up to 64 M144K (144K-bit) RAM blocks
 - Up to 10,624 MLAB (320-bit) RAM blocks
 - A 512 MB DDR2 memory with **4 GB/s** sustained throughput using up to 8 ports. (Up to 16 ports with lower access rate)
 - 2 DDR2 SODIMMs with up to **4 GB** each at a maximum sustained throughput of **8 GB/s**
 - Onboard SRAM options on SODIMM modules
- Supports Proc104 Daughter Boards:
Camera Links, SDI, User's Ethernet and other interfaces
 - Typical system frequencies: 100-325 MHz
 - Flexible clocking system
 - Volatile and non-volatile design security
 - Supported by GiDEL's *Proc Developer's Kit*
 - Supported by Windows and Linux Operating System

Benefits

- Leading edge performance
- Advance development tools
- Low power consumption
- Maintainability
- Reliability
- Long life cycle



Overview

The *Proc104*™ system provides a high-capacity, high-speed FPGA-based platform fortified with high throughput and massive memory, resulting in a powerful and highly flexible system. The *Proc104* complies with **PCIe/104**™ standard incorporating compact, self-stacking and rugged industrial-standard connectors. This powerful platform is ideal for high performance FPGA development and deployment across a range of SWaP-constrained application areas, including signal intelligence, image processing, software-defined radio and autonomous modules/vehicles.

The *Proc104* can be hosted via 4-lane PCI Express. The board's high speed performance coupled with memory and add-on daughter boards' flexible architecture enable the system to meet almost any computational needs. In addition to 512MB on-board memory, two SODIMM sockets provide up to 8GB of memory. Abundant memory conjoined with fast PCIe connection enable strong co-processing between a standard PC operating system and the Proc104's FPGA.

The *Proc104* system, with GiDEL's *Proc Developer's Kit* and tools, offers incredible performance yet supports quick implementation of your unique design. These unique features are achieved by eliminating the need for a high-speed board design, a PCI Express application driver, board constraints implementation, and environment FPGA code.

Target Applications

SWaP-Constrained industrial applications including:

- COTS acquisition and accelerator boards in:
 - ✓ HPC (High Performance Computing)
 - ✓ Machine Vision and Imaging
 - ✓ High performance acquisition systems
 - ✓ Bioinformatics Applications
- SW defined radio and autonomous modules/vehicles
- Small ASIC and SoC Prototyping
- Complex algorithm and IPs validation.

Development Environment

The *ProcDeveloper's Kit*, GiDEL's intuitive design and debug environment, facilitates design development effort on the *Proc104* system. The kit contains the *ProcWizard*[™] development software, GiDEL IPs including the innovative *ProcMultiPort*[™] IP memory controller, *Quartus*, *USBBlaster*, and the *Proc_HILs*[™] hardware-in-the-loop option.

The *ProcWizard* performs hardware initialization and automatically generates the following:

- Interface documentation in HTML or Microsoft Word.

- C++ class(es) application driver(s) enable simultaneous accesses of multiple applications, each to its' dedicated section of the Proc board. Top-level designs, interface modules/entities and on-board memory controllers for application use.
- Device constraints (as pin-outs).

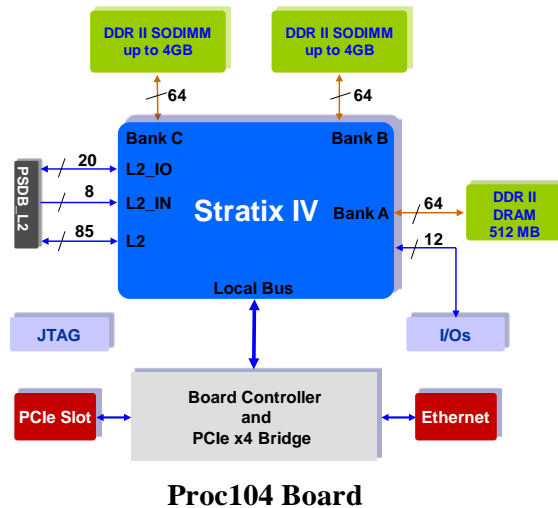
The *ProcMultiPort* and other memory control IPs provides simple access as FIFOs and frame delays to the on-board DRAM. It enables parallel access to the on-board memory while enabling to split the physical memory into multiple logical memories. As a result the main benefits are:

- Simplifies design and enhances system performance.
- Replaces the need for inventory of special memories by using standard memory and IP.

The *USBBlaster* enables visibility of internal signals using the available FPGA memory.

The *ProcHILs*[™] enables to accelerate *Simulink*[™] design simulation by implementing hardware-in-the-loop simulation on the *Proc104* board. Alternatively, the *ProcHILs* may be used, via Simulink, as a design entry tool for an FPGA based accelerator.

Other high-level design entry options, such as C++, are available via GiDEL's partners.



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